

WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit device comprising:

5 a register circuit which receives a data signal, an output timing of the register circuit being controlled by a clock signal;

10 a delay adjustment circuit which receives an output of the register circuit, a delay time of the delay adjustment circuit being adjusted by a delay adjustment signal based on the data signal; and

a driver circuit which receives an output of the delay adjustment circuit.

15 2. The device according to claim 1, wherein the data signal is a read data signal, and the driver circuit is an off-chip driver circuit.

3. The device according to claim 1, wherein the data signal is a write data signal, and the driver circuit is a write data buffer circuit.

20 4. The device according to claim 1, wherein the data signal is an address signal, and the driver circuit is an address buffer circuit.

5. A semiconductor integrated circuit device comprising:

25 a delay adjustment circuit which receives a clock signal, a delay time of the delay adjustment circuit being adjusted by a delay adjustment signal based on a data signal;

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a register circuit which receives the data signal,  
an output timing of the register circuit being  
controlled by a clock signal which is delay adjusted in  
the delay adjustment circuit; and

5 a driver circuit which receives an output of the  
register circuit.

6. The device according to claim 5, wherein the  
clock signal is a clock to output a read data, the data  
signal is a read data signal, and the driver circuit is  
10 an off-chip driver circuit.

7. A semiconductor integrated circuit device  
comprising:

register circuits which receive data signals,  
an output timing of each of the register circuits being  
15 controlled by a clock signal;

delay adjustment circuits which receive outputs  
of the register circuits, a delay time of each of the  
delay adjustment circuits being adjusted by a delay  
adjustment signal based on the data signals adjacent to  
20 each other; and

driver circuits which receive outputs of the delay  
adjustment circuits.

8. The device according to claim 7, wherein the  
data signals are read data signals, and the driver  
25 circuits are off-chip driver circuits.

9. The device according to claim 7, wherein the  
data signals are write data signals, and the driver

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circuits are write data buffer circuits.

10. The device according to claim 7, wherein the data signals are address signals, and the driver circuits are address buffer circuits.

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